

FURBER, S.  
Appl. No. 10/509,086  
September 24, 2007

**AMENDMENTS TO THE DRAWINGS**

Proposed drawing changes are shown on the attached annotated marked up drawing and are incorporated within an attached proposed replacement sheets of drawings.

**REMARKS/ARGUMENTS**

Reconsideration of this application is respectfully requested.

In response to the rejection of claim 21 under 35 U.S.C. §112, second paragraph, the word “substantially” has been removed from claim 21 as suggested by the Examiner.

The rejection of claims 1, 6, 16-21, 23 and 30-31 under 35 U.S.C. §102 as allegedly anticipated by Ichiriu ‘595 is respectfully traversed.

It is central to the claimed invention (e.g., see each of independent claims 1, 15, 16 and 21) that a plurality of address decoders are provided and that a particular address decoder is activated if but only if a predetermined minimum number of bits set to the first selectable state (e.g. “1”) in the input address correspond to bits set to the first selectable state (e.g. “1”) in the decoder identifier. This is perhaps best described in the specification with reference to simplified examples at pages 13 and 14.

The Examiner refers primarily to Figure 2 of Ichiriu which does describe an address selector 125. The address selector 125 selects one of a plurality of address sources (121, 122, 124) so as to output a selected address 178. It is to be noted that the address selection described in Ichiriu is based upon the select signal 118 not upon any comparison between an identifier of the address decoder and the input address.

The Examiner contends that use of “additional address sources” as referenced by Ichiriu discloses the use of a plurality of address decoders. This is incorrect. If the address selector 125 is to be considered an address decoder it is clear that the address decoder 125 selects from a plurality of address sources. That is, address sources are input to address selector 125 and it is wrong to contend that the address sources are themselves address decoders. Thus, it is clear that

the limitation of claim 1 requiring a plurality of address decoders is neither taught nor suggested by Ichiriu.

Similarly, it is clear that the address selector 125 of Ichiriu does not have an identifier having a predetermined number of bits. Indeed, no identifier associated with the address selector 125 is taught or suggested. Given the way in which the address selector 125 operates based upon the select signal 118 it is clear that an identifier associated with the address selector 125 would serve no useful purpose in the described system.

Further, there is nothing in Ichiriu to teach or suggest means to compare the identifier of an address decoder with the input address. Indeed, this follows given the absence of an identifier from the address selector of Ichiriu.

The Examiner's inherency argument is based upon a compare operation described at column 5 lines 22 to 26. It is clear that this compare operation is concerned with the loading of a highest priority match register 125. It is further clear that this comparison operation has nothing to do with an address input to the address selector nor with an identifier of the address selector.

Finally, as indicated above, the address selector 125 of Ichiriu selects an input address based upon select signal 118. There is therefore nothing in Ichiriu to teach or suggest activating an address decoder if at least a predetermined minimum number of bits is set in some manner-- i.e., such that the first selectable state in the input address correspond to bits set to the first selectable state in the decoder identifier. It is to be noted that the Examiner again refers to column 5 lines 22 to 26 when this passage does not even involve the address selector 125 of Ichiriu.

Considering claim 21, Ichiriu does not teach a method for optimizing the operation of a computer memory. Many of the comments made with regard to claim 1 similarly apply to claim

21. Specifically, there is nothing in Ichiriu to teach a plurality of address decoders and there is nothing to indicate that the address decoders are allocated an identifier. The reasoning for these positions is set out above with reference to claim 1. Furthermore, there is nothing in Ichiriu to teach means to activate one or more of the address decoders as a comparison between a decoder identifier and the input address exceeds a predetermined comparison threshold.

The Examiner's position with regard to Ichiriu teaching determination of an operationally beneficial number of address decoders to be activated is also clearly erroneous. Given that there is only a single address decoder, the Examiner's reasoning is fundamentally flawed leading to an erroneous conclusion that claim 21 is anticipated.

Given such fundamental deficiencies of Ichiriu with respect to rejected independent claims 1, 16 and 21, it is not believed necessary at this time to note the additional deficiencies of this reference with respect to other features of the independent claims and with respect to the additional features brought in by the rejected dependent claims. Suffice it to note that, as a matter of law, it is impossible for a reference to anticipate a claim unless that reference teaches every feature of the rejected claim.

The rejection of claim 15 under 35 U.S.C. §102 as allegedly anticipated by Thewes '626 is also respectfully traversed.

With regard to claim 15, the Examiner's assertion that "it is widely known in the art that an address decoder is a multiplexor" is wrong. This error forms the basis for the Examiner's entire rejection of claim 15. If the Examiner intends to maintain this position it is requested that this assertion be supported by evidence. Given that Thewes does not even relate to an address decoder it is nothing more than peripheral relevance to the invention of claim 15.

The rejection of claims 2-5, 7-12 and 22 under 35 U.S.C. §103 as allegedly being made "obvious" based on Ichiriu in view of Mano is also respectfully traversed.

Fundamental deficiencies of Ichiriu have already been noted above with respect to a parent claim. Those deficiencies are not supplied by Mano. Accordingly, it is not believed necessary at this time to detail the additional deficiencies of this allegedly "obvious" combination of references with respect to other features of these rejected dependent claims.

The Examiner's indication of allowable subject matter at claims 24-29 is appreciatively noted. No further comment will be made with respect to any of these claims.


The Examiner's attention is also drawn new claims 35 and 36. These claims are respectively based upon claims 1 and 16 but have been slightly amended to make clear that each of the address decoders selects only a predetermined one of the plurality of word lines. That is, these claims require a 1-to-1 relationship between an address decoder and the word line which it activates. This also is a clearly different system from any taught by the prior art.

Accordingly, this entire application is now believed to be in allowable condition and a formal notice to that effect is earnestly solicited.

Respectfully submitted,

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ANNOTATED MARKED UP DRAWINGS  
FOR SN 10/509,086

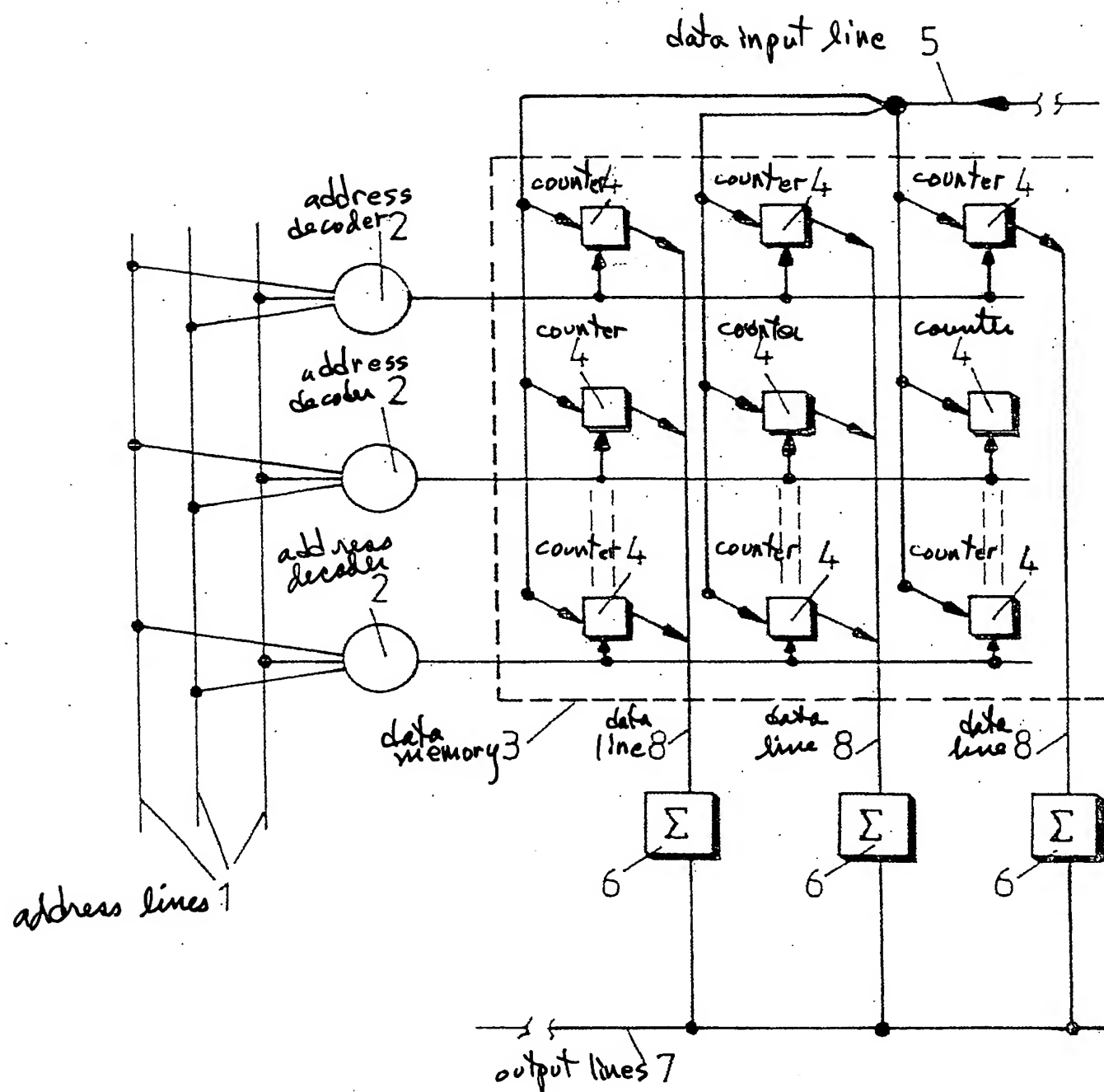


FIG. 1  
(PRIOR ART)

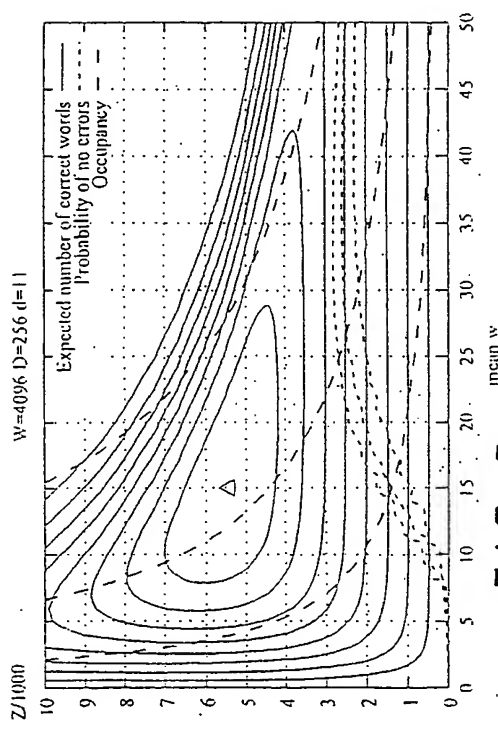


FIG.5

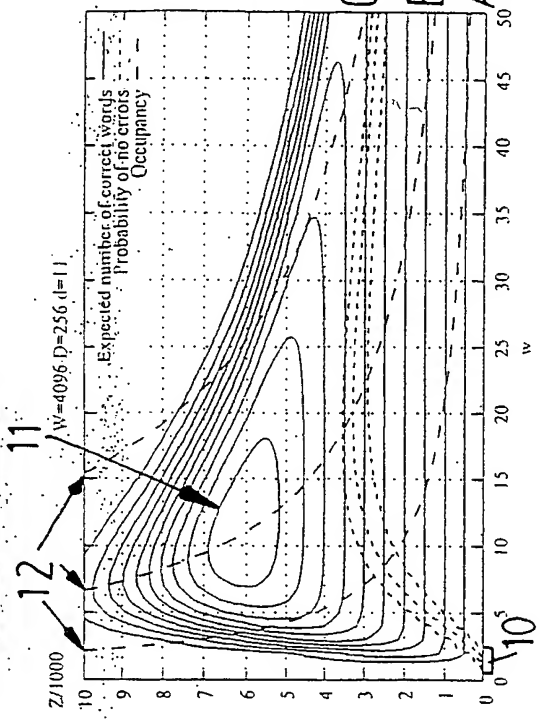


FIG.4

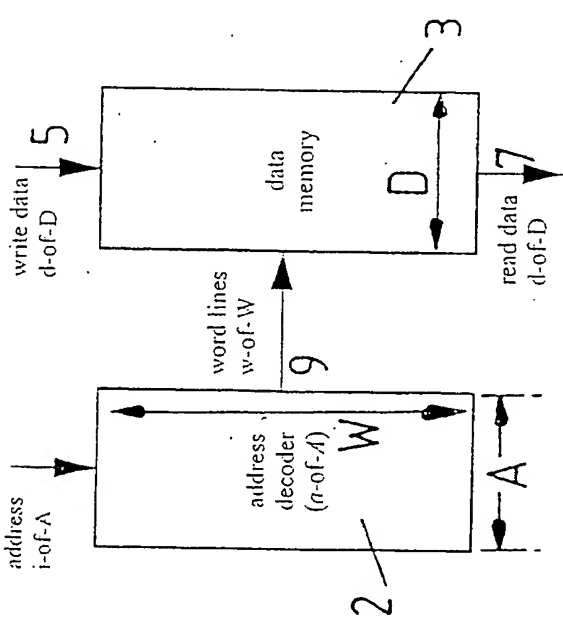


FIG.2

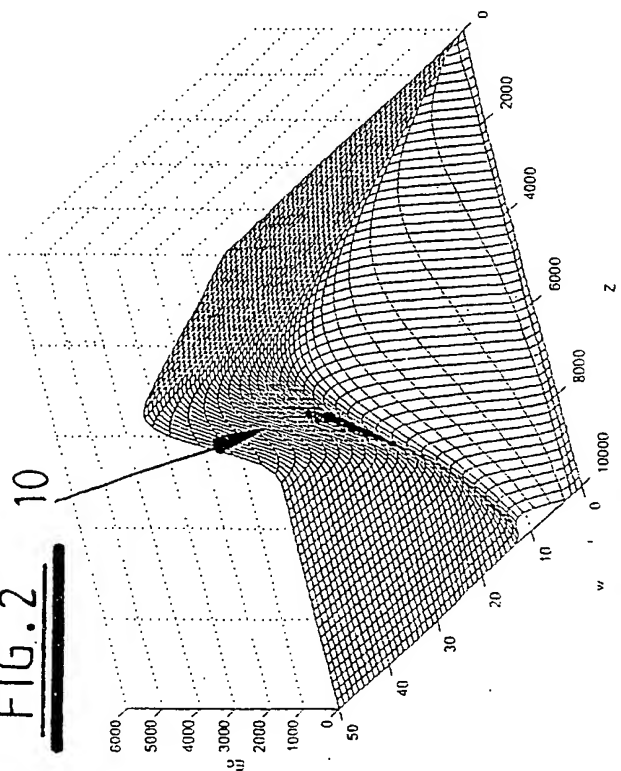


FIG.3

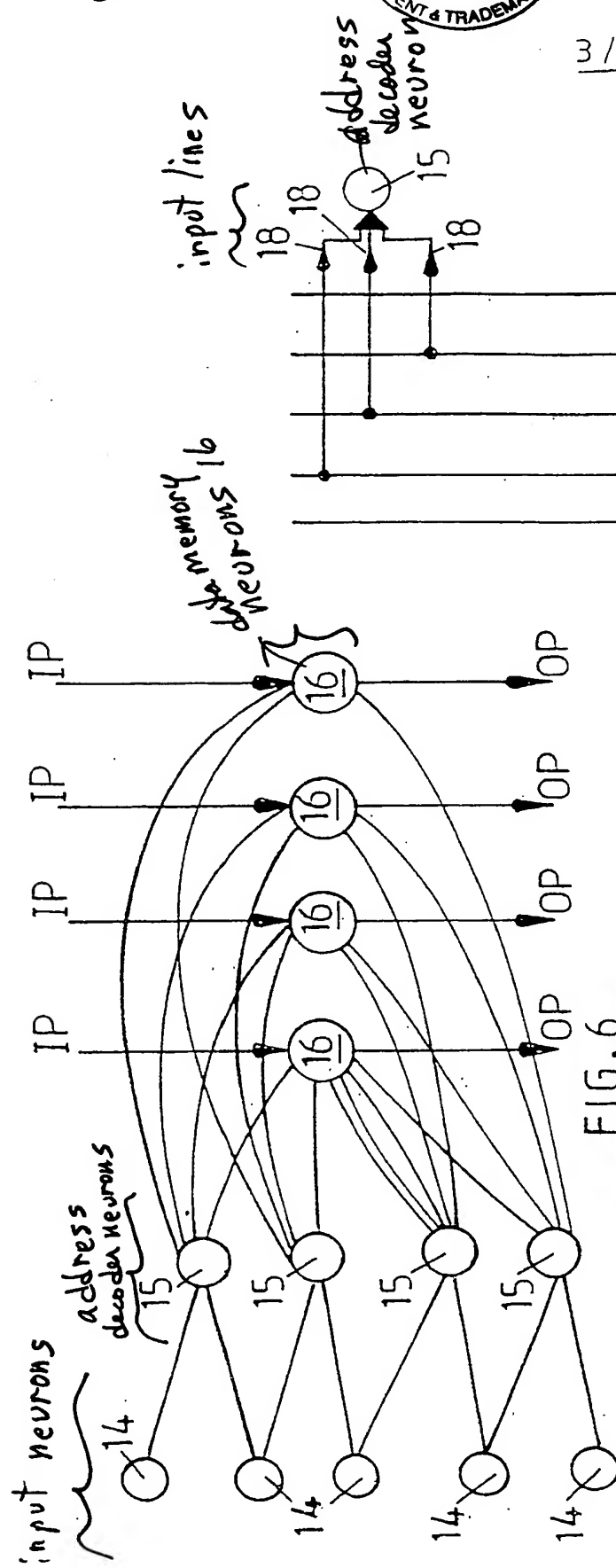


FIG. 6

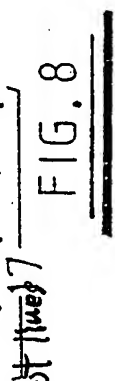


FIG. 7

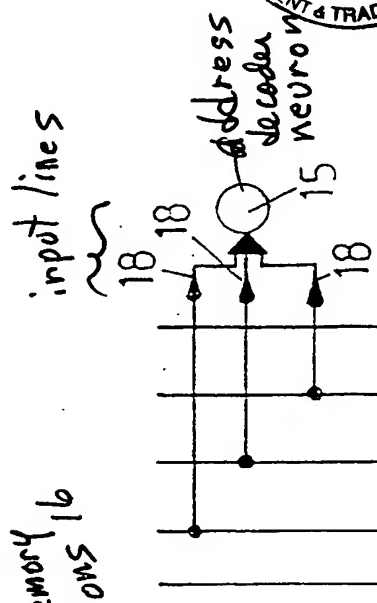


FIG. 8